Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Canceled)

6. (Previously Presented) The non-volatile semiconductor memory according to claim 20, wherein said side wall comprises a first side wall and a second side wall formed on the first side wall, and wherein an end of said drain region and an end of said first sidewall, and an end of said source region and an end of said second side wall are in predetermined positional relations.

7-18. (Canceled)

19. (Currently Amended) A non-volatile semiconductor memory comprising:

a semiconductor substrate;

a source region provided in said semiconductor substrate;

a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other with a channel region disposed therebetween;

a floating gate provided above ~~a~~ said channel region ~~between said source and drain regions~~; and

a control gate provided above said channel region;

wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said floating gate,

and an erasing operation is performed by releasing the electrons held by said floating gate into said channel region;

wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate;

wherein said floating gate is provided between said channel region and said control gate through respective insulating layers; and

wherein a junction depth of said source region is larger than a junction depth of said drain region.

20. (Previously Presented) The non-volatile semiconductor memory according to claim 19, wherein at least said source region has an end having a predetermined positional relation with an end of a side wall provided on a side surface of said control gate.

21. (Currently Amended) A non-volatile semiconductor memory comprising:

a semiconductor substrate;

a source region provided in said semiconductor substrate; and

a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other with a channel region disposed therebetween;

a control gate provided above said channel region; and

~~wherein a~~ an electric charge accumulation portion that is an insulating layer having a trap level therein, ~~and~~ said insulating layer ~~is~~ being provided between said channel region and control gate ~~and said control gate is provided above said channel region~~;

wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said electric charge accumulation ~~region~~ portion and ~~the~~ an erasing operation involves neutralization of the electrons held by the trap level by injecting holes generated ~~at~~ in the vicinity of said drain region;

wherein an overlap of said drain region with said electric charge accumulating portion is set larger than an overlap of said source region with said electric charge accumulating portion; and

wherein a junction depth of said source region is larger than a junction depth of said drain region.

22. (Previously Presented) The non-volatile semiconductor memory according to claim 21, wherein at least said source region has an end having a predetermined positional relation with an end of a side wall provided on a side surface of said control gate.

23. (Canceled)

24. (Previously Presented) The non-volatile semiconductor according to claim 22, wherein said side wall comprises a first side wall and a second side wall formed on the first side wall, and wherein and end of said drain region and an end of said first sidewall and an end of said source region and an end of said second side wall have predetermined positional relations.

25. (New) The non-volatile semiconductor memory according to claim 19, wherein said erasing operation releases electrons over a width of said channel region between said source and drain regions.

26. (New) The non-volatile semiconductor memory according to claim 19, wherein said erasing operation releases electrons to said channel region regardless of position with respect to said source and drain regions.

27. (New) The non-volatile semiconductor memory according to claim 19, wherein said source region is formed self-aligned to a side wall provided on a side surface of said control gate.

28. (New) The non-volatile semiconductor memory according to claim 27, wherein said side wall comprises a first side wall and a second side wall formed on the first side wall.

29. (New) The non-volatile semiconductor memory according to claim 6, wherein said drain region is substantially aligned with said first sidewall and said source region is substantially aligned with said second side wall.

30. (New) The non-volatile semiconductor memory according to claim 19, further comprising circuitry to set a control gate potential to a relatively low potential compared to a channel potential and to set said channel potential to a relatively high, positive potential compared to said control gate potential, thereby conducting said erasing operation.

31. (New) The non-volatile semiconductor memory according to claim 30, wherein the channel potential is provided through a contact to a p-well.

32. (New) The non-volatile semiconductor memory according to claim 21, wherein said erasing operation releases electrons over an entire surface of said channel region.

33. (New) The non-volatile semiconductor memory according to claim 21, wherein said source region is formed self-aligned to a side wall provided on a side surface of said control gate.

34. (New) The non-volatile semiconductor memory according to claim 24, wherein said drain region is substantially aligned with said first sidewall and said source region is substantially aligned with said second side wall.

35. (New) The non-volatile semiconductor memory according to claim 21, further comprising circuitry to accomplish said erase operation by increasing a drain region potential with respect to a source region potential and by decreasing a control gate potential with respect to said source region potential.